WHAT IS CLAIMED IS:

1. A flip chip semiconductor device comprising a silicon wafer having parallel first and second major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second coplanar, laterally spaced and metallized areas formed on said first major surface and insulated from one another and connected to said P region and said N region respectively; said second major surface being intentionally roughened to define an extended area for improved convection cooling for said semiconductor device.

2. A flip chip semiconductor device comprising a silicon wafer having parallel first and second major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second coplanar, laterally spaced and metallized layers formed on said first major surface and insulated form one another and connected to said P region and said N region respectively; and a bottom metallized layer extending across said second major surface.

3. The device of claim 1 which includes a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device.

4. The device of claim 2 which includes a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device.

5. The device of claim 1 which further includes at least one contact bump connected to each of said metallized layers.

6 The device of claim 2 which further includes at least one contact bump connected to each of said metallized layers.

7. The device of claim 3 which further includes at least one contact bump connected to each of said metallized layers.

8. The device of claim 4 which further includes at least one contact bump connected to each of said metallized layers.

9. The device of claim 2 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

10. The device of claim 4 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

11. The device of claim 6 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

12. The device of claim 8 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

13. The device of claim 5 wherein a plurality of contact bumps are connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallized layer being aligned along a first straight

row; said plurality of contact bumps connected to said second metallized layer being aligned along a second straight row.

14. The device of claim 13 wherein said first and second rows are parallel to one another.

15. The device of claim 6 wherein a plurality of contact bumps are connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallized layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallized layer being aligned along a second straight row.

16. The device of claim 15 wherein said first and second rows are parallel to one another.

17. The device of claim 13 which includes a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device.

18. The device of claim 14 which includes a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device.

19. A flip chip semiconductor device comprising a silicon wafer having first and second parallel major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and

second coplanar, laterally spaced metallized layers formed on said first major surface and insulated form one another and connected to said P region and said N region respectively; and a plurality of contact bumps connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallizing layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallizing layer being aligned along a second straight row.

20. The device of claim 19 which includes a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallizing layers comprising source, drain and gate electrodes respectively of a MOSgated device.

21. The device of claim 19 and a bottom metallized layer extending across said second major surface.

22. The device of claim 19 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

23. The device of claim 19 wherein said first and second rows are parallel to one another.

24. The device of claim 19 wherein said silicon wafer is a rectangular wafer having an area defined by a given length and a given width, said length being greater than said width; said first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across said wafer.

25. The device of claim 24 which includes a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device.

26. The device of claim 21 wherein said silicon wafer is a rectangular wafer having an area defined by a given length and a given width, said length being greater than said width; said first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across said wafer.

27. The device of claim 19 which further includes a bottom metallized layer extending across said second major surface.

28. A bidirectional conduction flip chip device comprising a silicon wafer having first and second parallel major surfaces; first and second laterally separated MOSgated devices formed in said silicon wafer; said first and second MOSgated devices comprising a first and a second source region respectively of one conductivity formed into a first and second spaced lateral area respectively of said first major surface, a first and second channel region respectively of a second conductivity type receiving said first and second source region, respectively a common drain region receiving said first and second channel regions and extending to said second major surface, and a first and second gate structure respectively disposed on said first major surface and operable to invert respective portions of said first and second channel regions to allow conduction from said first and source regions respectively to said drain region; first and second laterally spaced source metallized layers disposed atop said first major surface and connected to said first and second source regions respectively; and first and second laterally spaced gate

metallized layers atop said first major surface and connected to said first and second gate structures respectively.

29. The device of claim 28 which further includes at least one contact bump connected to each of said source and gate metallized layers.

30. The device of claim 29 which includes a respective plurality of contact bumps connected to each of said source metallized layers; each of said plurality of contact bumps arranged in respective spaced rows which are parallel to one another.

31. The device of claim 28 wherein said first and second source regions are disposed in laterally interdigitated relation with respect to one another.

32. The device of claim 30 wherein said first and second source regions are disposed in laterally interdigitated relation with respect to one another.

33. The device of claim 28 which further includes a metal layer on said second major surface.

34. A semiconductor device comprising a silicon die having first and second parallel surfaces; a region of one conductivity type extending from said first surface and into the body of said die; a junction pattern defined in said device formed by a plurality of laterally spaced diffusions of the other conductivity type into said region of one conductivity type; a first conductive electrode formed atop said first surface and in contact with said first plurality of diffusions; a second conductive electrode formed atop said first surface which is coplanar with and laterally spaced from and insulated from said first conductive electrode and in contact with said

region of one conductivity type; and at least one solder ball connector formed atop each of said first and second conductive electrodes respectively; the current path from said first conductive electrode to said second conductive electrode having a vertical component which is generally perpendicular to said first surface.

35. The device of claim 34 wherein said device comprises a power MOSgated device; said first and second electrodes comprising the main power electrodes of said device.

36. The device of claim 35 wherein said device includes a polysilicon gate structure formed adjacent said plurality of diffusions and operable to turn said device on and off, and a third conductive electrode formed atop said first surface and coplanar with and laterally spaced from and insulated from said first and second conductive electrodes and connected to said polysilicon gate structure; and a solder ball connector connected to said third conductive electrode; all of said solder ball connectors being coplanar with one another.

37. The device of claim 36 wherein said device is a flip-chip power MOSFET.

38. The device of claim 34 wherein said one conductivity type is the P type.

39. The device of claim 36 wherein said one conductivity type is the P type.

40. The device of claim 34 wherein said region of one conductivity type includes an upper layer of relatively low concentration expitaxially formed silicon and a lower layer of higher concentration non-epitaxial silicon.

41. The device of claim 36 wherein said region of one conductivity type includes an upper layer of relatively low concentration expitaxially formed silicon and a lower layer of higher concentration non-epitaxial silicon.

42. The device of claim 40 which further includes a sinker diffusion of relatively high concentration extending from and connected to said second electrode to said lower layer of said region.

43. The device of claim 41 which further includes a sinker diffusion of relatively high concentration extending from and connected to said second electrode to said lower layer of said region.

44. The device of claim 40 which further includes a trench extending through said upper layer of said region of one conductivity type and a conductive material which at least lines the side walls of said trench.

45. The device of claim 44 wherein said device includes a polysilicon gate structure formed adjacent said plurality of diffusions and operable to turn said device on and off, and a third conductive electrode formed atop said first surface and coplanar with and laterally spaced from and insulated from said first and second conductive electrodes and connected to said polysilicon gate structure; and a solder ball connector connected to said third conductive electrode; all of said solder ball connectors being coplanar with one another.

46. The device of claim 43 wherein said device is a flip-chip power MOSFET.

47. The device of claim 45 wherein said device is a flip-chip power MOSFET.

48. The device of claim 46 wherein said one conductivity type is the P type.

49. The device of claim 47 wherein said one conductivity type is the P type.

50. The device of claim 36 wherein said second surface is roughened to define an extended area for improved cooling of said device.

51. The device of claim 36 which further includes a metal layer secured to and extending across said second surface.

52. The device of claim 34, wherein said device is selected from the group consisting of MOSFETs, Schottky diodes, bipolar transistors, and P/N diodes.

53. The device of claim 34, wherein said solder balls are arranged on a pitch greater than about 0.8 mm and have diameters greater than about 200 μ.

54. The device of claim 52, wherein said solder balls are arranged on a pitch greater than about 0.8 mm and have diameters greater than about 200 μ.